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10/528,328	09/15/2005	Andrew Kay	YAMAP0971US	6767

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	**PAPER NUMBER**
2117	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/528,328	KAY, ANDREW	
	Examiner	Art Unit	
	STEVEN D. RADOSEVICH	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-31 are present within this instant examination, which is in response to applicant's response to the initial examination mailed to the applicant on 3/26/2008. Examiner notes that claim 16 has been canceled by the applicant and therefore will not be given further consideration within this instant examination.

Priority

Priority as noted within the prior examination is acknowledged to 9/20/2002.

Information Disclosure Statement

Examiner notes that WO 00068794 as indicated within the prior IDS was not considered as indicated by the applicant within applicant's response since it is not in English. However WO 00068794 does have a U.S. Patented Patent Family member, U.S. Patent 6622205, which has been considered since it is in English; leaving the WO 00068794 itself still not considered but the contents considered since the contents are believed to be disclosed within the U.S. Patented Patent Family member, U.S. Patent 6622205, reviewed and considered. Examiner can not consider what examiner can not read or understand (non-English documents).

Response to Arguments

Applicant's arguments, filed 6/26/2008, with respect to the claim objections and 35 U.C.S. 101 rejections have been fully considered and are persuasive. Therefore the prior Claim objections and 101 rejections of claims 1, 11, 13, and 14-15 respectively made within the prior examination has been withdrawn in view of applicant's amendments.

Applicant's arguments filed 6/26/2008 have been fully considered but they are not persuasive with respect to the 35 U.S.C. 112 second paragraph rejections and therefore the 35 U.S.C 102 and 103 rejections. Applicant argues the following:

i. With respect to the 35 U.S.C. 112 second paragraph rejections: That the claims are definite and therefore withdrawal of the rejection is requested, referencing figure 3 and providing the following example to provide explanation that the claims are definite:

"During the initial write operation a first value (value data 0) is stored at PDI node 30, and the last word of this node (the pointer field 31) is at address 0014. Additionally, a pointer to the last word of node 30 is stored in the PDI table 9.

During the second write operation for value data 1, the computer 2 finds the pointer for the PDI in table 9 and checks the pointer field 31 to discover that the node 30 contains the immediately preceding value of the PDI. The next value (value data 1) then is written into the value field of node 32 and the address 1234 is entered into the pointer field at node 30, and the counter 10 is updated.

During the third write operation, the computer 2, based on the pointers, determines that node 32 contains the immediately preceding value. The next available space for a node in the memory segment is located and a node is allocated with its pointer field at address 2200. Allocation of the node is performed by changing the lowest bit of the

address 2200 to 0, thus leaving FFFE in the pointer field. The value data 2 is stored in the value field of node 33 and the next non-zero bit of the counter 10 is set to 0. A pointer to node 33 then begins to be written into the pointer field of node 32 but prior to completion, power is removed, resulting in an incompletely written pointer (e.g. 2274 is written in the pointer field of node 32).

When power is the next applied to the memory card 1, the routine shown in figure 4 is performed. This determines that the address field of node 33 is stored at the LUM (which is 220). This value is compared to the address stored in the pointer filed 32 (which is 2274). Since address in the pointer field 32 (which, is the present example, corresponds to the "determined address" of claim 1) is not in the range of the memory block that includes the LUM (in this example, 2274 is not in the range of 220), it is concluded that the third write operation failed."

With respect to applicant's arguments and Example the Examiner would like to further explain the issues that make the claims indefinite by directing the applicant specifically the two issues within the claims and one within the applicant provided example:

Claims:

(1) That the "address range" of the memory block including the last new memory location (LUM) is not specifically defined and therefore to one of ordinary skill within the art represents the **entire**

address range of the memory (i.e. 0000-to-1111, wherein the memory block has a range of 16 addressable locations), and therefore would include all the addresses of the memory leaving none outside the address range thus never performing the claimed action.

(2) The "an action" being performed is not specifically defined and therefore to one or ordinary skill within the art represents any action performed.

Example:

(3) The example does as described with the values provided by the applicant perform that which applicant has argued. However the example is not always true or a given. The Examiner would like provide applicant the same example to support this understanding, wherein with respect to the pointer field within node 32 being written to when power is removed the incompletely written pointer is 2000 (not 2274); the pointer 2000 is within the range of 2200, and therefore no action is performed. The Examiner provided example illuminates the issue/fact that within the example the contents within node 32 being written to when power is removed is unknown and therefore may or may-not be within a defined address range including the last new memory location, and therefore may or may-not result in an action being performed.

In view of the above provided explained issues per the claims that further explain the grounds of the prior 35 U.S.C. 112 second paragraph rejections that leave the claim indefinite/unclear and to the Examiner's best broadest reasonable interpretation (M.P.E.P. 2111) as to that which is being claimed, and to the above provided Examiner's example and explanation, the prior 35 U.S.C. 112 second paragraph rejections are maintained. The rejections are maintained since the issues remain with the claims that render the claims indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards at the invention.

Furthermore the U.S.C. 102 and 103 rejections are also maintained since the best broadest reasonable interpretation of the claims were/are being used within the examination of the claims in conjunction with 2111 of the M.P.E.P. in view of the 35 U.S.C. 112 second paragraph rejections.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8, 11-13, 17-22, 24, and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Teich et al (U.S. Publication 20010007108 A1, filed 12/22/2000 and published 7/5/2001).

1. As per claims 1, 17, and 31, Teich teaches a method of detecting an error in a persistent memory segment in which values of at least one data item are stored in

temporally consecutively allocated locations, each new memory location is added to a first end of a block of the memory segment having first and second ends, and a pointer to each new memory location is added to an older memory location in the block containing a preceding value of the at least one data item (Linked list and EEPROM: paragraph 0049, abstract, and figures 3A-B), the method being characterized by comprising:

a. determining the address to which the last-added pointer points (new (current) record is 'active' in paragraph 0073);

b. comparing the determined address with an address range of the memory block including the last new memory location (LUM) (paragraph 0073 with respect to the previous record is 'fully active' and paragraphs 0062-0063 with 0066-0067) ; and

c. performing an action if the determined address is outside the address range (modify in paragraph 0075).

2. As per claims 2 and 18, Teich teaches wherein the steps (a) to (c) are performed each time power is applied to the memory segment (paragraph 0068.

3. As per claims 3 and 19, wherein the step (a) comprising determining the addresses to which all of the pointers point and selecting the highest or lowest address (new (current) record in paragraph 0073 and last appended (current record in paragraph 0062).

4. As per claims 4 and 20, wherein the step (c) comprises changing the address of the last-added pointer to the address of the last new memory location ('fully active' in paragraph 0075).

5. As per claims 5 and 21, wherein each new memory location is added contiguously to the first end of the block (linked list in paragraph 0069, and 0049, and figures 3A-B).

6. As per claims 6 and 22, wherein each pointer points to a highest or lowest address of the memory location to which it points linked list in paragraph 0069, and 0049, and figures 3A-B).

7. As per claims 8 and 24, wherein each memory location has space for a single value of the at least one data item (data in paragraphs 0009-0010, linked list in paragraphs 0049 and 0069, and figures 3A-B).

8. As per claims 11, 12, 27, and 28, wherein the memory segment contains at least one write counter in which a respective flag is set at the end of each value storing operation and a respective further flag is set at the end of each pointer adding operation, and also characterized in that the steps (a) to (c) are performed only if an odd number of flags and further flags is set ('active' and 'fully active' in paragraphs 0072-0079).

9. As per claims 13 and 29, wherein the memory segment contains at least one write counter in which, when storing a series or one or more data item values, a respective flag is set before the first pointer adding operation in the series and a respective further flag is set after the final pointer adding operation in the series, and

also characterized in that the steps (a) to (c) are performed only if an odd number of flags and further flags is set ('active' and 'fully active' in paragraphs 0072-0079).

10. As per claim 30, Teich teaches comprising a smart card (chip cards in paragraph 0003).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7, 9, 10, 23, 25, and 26, are rejected under 35 U.S.C. 103(a) as being unpatentable over Teich et al (U.S. Publication 20010007108 A1) as applied to claims 1 and 17 respectively above, and further in view of AAPA (Applicants Admitted Prior Art within U.S. Publication 20060143541 A1).

11. As per claims 7 and 23, Teich teaches as described above lined list with power failure and subsequent recovery dealing with EEPROM memory (title, abstract, and paragraph 0011).

Teich does not specifically teach wherein the memory segment comprises at least part of a flash memory.

AAPA teaches within the background art that EEPROM and Flash memory are different variations of RAM (paragraph 0004).

Therefore one of ordinary skill within the art at the time the invention was made could have been motivated to modify Teich so as to replace the EEPROM with Flash memory since as indicate within AAPA they are both types of RAM and thus equally applicable wherein RAM is used.

12. As per claims 9 and 25, Teich teaches as described above lined list with power failure, subsequent recovery dealing with EEPROM memory, and the action is performed when the detected address is greater than the highest address of the address range (paragraph 0075 and figures 3A-B).

Teich does not specifically teach wherein each bit of the memory segment is individually switchable only from 1 to 0.

AAPA teaches memory individually switchable only from 1 to 0 (paragraph 0010).

Therefore one of ordinary skill within the art at the time the invention was made could have been motivated to have the memory within Teich individually switchable only from 1 to 0 as AAPA teaches since a memory must have a base/reset/clear/erased

value/state as AAPA teaches (paragraph 0010) and switchable only from 1 to 0 is a well known proven and reliable way to write date onto a memory.

13. As per claims 10 and 26, Teich teaches as described above lined list with power failure, subsequent recovery dealing with EEPROM memory, and the action is performed when the detected address is less than the highest address of the address range (paragraph 0075 and figures 3A-B).

Teich does not specifically teach wherein each bit of the memory segment is individually switchable only from 0 to 1.

AAPA teaches memory individually switchable only from 1 to 0 (paragraph 0010) as noted above.

Therefore one of ordinary skill within the art at the time the invention was made could have been motivated to have the memory within Teich individually switchable only from 0 to 1 as since a memory must have a base/reset/clear/erased value/state switchable/changeable for writing as AAPA teaches (paragraph 0010), and it would have been obvious to one having ordinary skill within the art at the time the invention was made to inverse the base/reset/clear/erased value/state form 1 as in AAPA to 0 since the examiner takes official notice of the equivalence of the base/reset/clear/erased value/state being a 1 (high) and a 0 (low) for their use in being the base/reset/clear/erased value/state of the memory and the selection of there known equivalents to be the base/reset/clear/erased value/state of the memory would be within the level of ordinary skill. Examiner notes the base/reset/clear/erased value/state within any binary system can only be either a 1 or a 0 as is well known within the art.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN D. RADOSEVICH whose telephone number is (571)272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner,
Art Unit 2117

Steven D. Radosevich
Examiner
Art Unit 2117